WHAT IS CLAIMED IS:

1. A clocked inverter comprising:

a first transistor and a second transistor connected in series, and

a compensation circuit comprising a third transistor and a fourth transistor connected in series, wherein:

gates of the third transistor and the fourth transistor are connected to each other,

drains of the third transistor and the fourth transistor are each connected to a gate of the first transistor,

sources of the first transistor and the fourth transistor are each electrically connected to a first power source,

a source of the second transistor is electrically connected to a second power source, and

an amplitude of a signal inputted to a source of the third transistor is smaller than a potential difference between the first power source and the second power source.

2. A clocked inverter according to claim 1, wherein:

the first power source is a high potential power source;

the second power source is a low potential power source;

the first transistor and the fourth transistor are each a P-type transistor; and

the second transistor and the third transistor are each an N-type transistor.

3. A clocked inverter according to claim 1, wherein:

the first power source is a low potential power source;

the second power source is a high potential power source;

the first transistor and the fourth transistor are each an N-type transistor; and

the second transistor and the third transistor are each a P-type transistor.

4. A clocked inverter according to claim 1, wherein the third transistor is replaced with an analog switch.

5. A clocked inverter comprising:

first to third transistors connected in series, and

a compensation circuit comprising a fourth transistor and a fifth transistor connected in series, wherein:

gates of the fourth transistor and the fifth transistor are connected to each other;

drains of the fourth transistor and the fifth transistor are each connected to a gate of the first transistor;

sources of the first transistor and the fifth transistor are each electrically connected to a first power source;

a source of the third transistor is electrically connected to a second power source; and

an amplitude of a signal inputted to a source of the fourth transistor is smaller than a potential difference between the first power source and the second power source.

6. A clocked inverter according to claim 5, wherein:

the first power source is a high potential power source;

the second power source is a low potential power source;

the first transistor and the fifth transistor are each a P-type transistor; and

the second to fourth transistors are each an N-type transistor.

7. A clocked inverter according to claim 5, wherein:

the first power source is a high potential power source;

the second power source is a low potential power source;

the first transistor, the second transistor, and the fifth transistor are each a P-type transistor; and

the third transistor and the fourth transistor are each an N-type transistor.

8. A clocked inverter according to claim 5, wherein:

the first power source is a low potential power source;

the second power source is a high potential power source;

the first transistor and the fifth transistor are each an N-type transistor; and

the second to fourth transistors are each a P-type transistor.

9. A clocked inverter according to claim 5, wherein:

the first power source is a low potential power source;

the second power source is a high potential power source;

the first transistor, the second transistor, and the fifth transistor are each an N-type transistor; and

the third transistor and the fourth transistor are each a P-type transistor.

10. A clocked inverter according to claim 5, wherein the fourth transistor is replaced with an analog switch.

11. A NAND comprising:

a first transistor and a second transistor connected in parallel;

a third transistor connected to the first transistor and the second transistor in series; and

a compensation circuit including a fourth transistor and a fifth transistor connected in series, wherein:

gates of the fourth transistor and the fifth transistor are connected to each other;

drains of the fourth transistor and the fifth transistor are each connected to a gate of the third transistor;

sources of the first transistor and the second transistor are each electrically connected to a high potential power source;

sources of the third transistor and the fifth transistor are each electrically connected to a low potential power source; and

an amplitude of a signal inputted to a source of the fourth transistor and each of gates of the first transistor, the second transistor, the fourth transistor, and the fifth transistor is smaller than a potential difference between the high potential power source and the low potential power source.

12. A NAND according to claim 11, wherein the first transistor, the second transistor, and the fourth transistor are each a P-type transistor, and the third transistor and the fifth transistor are each an N-type transistor.

13. A NAND according to claim 11, wherein the fourth transistor is replaced with an analog switch.

14. A NOR comprising:

a first transistor and a second transistor connected in parallel;

a third transistor connected to the first transistor and the second transistor in series; and

a compensation circuit including a fourth transistor and a fifth transistor connected in series, wherein:

gates of the fourth transistor and the fifth transistor are connected to each other;

drains of the fourth transistor and the fifth transistor are each connected to a gate of the third transistor;

sources of the first transistor and the second transistor are each electrically connected to a low potential power source;

sources of the third transistor and the fifth transistor are each electrically connected to a high potential power source; and

an amplitude of a signal inputted to each of gates of the first transistor, the second transistor, the fourth transistor, and the fifth transistor and to a source of the fourth transistor is smaller than a potential difference between the high potential power source and the low potential power source.

15. A NOR according to claim 14, wherein the first transistor, the second transistor, and the fourth transistor are each an N-type transistor, and the third transistor and the fifth transistor are each a P-type transistor.

16. A NOR according to claim 14, wherein: the fourth transistor is replaced with an analog switch.

17. A shift register comprising:

a clocked inverter including a first transistor to a third transistor connected in series; and

a compensation circuit including a fourth transistor and a fifth transistor connected in series, wherein:

sources of the first transistor and the fifth transistor are each electrically connected to a first power source;

a source of the third transistor is electrically connected to a second power source;

a gate of the first transistor is connected to an output terminal of the compensation circuit;

a pulse generated at an (n-1)th stage is inputted to an input terminal of the compensation circuit arranged at an n-th stage; and

a pulse or a clock signal generated at an (n-2)th stage is inputted to a source of the fourth transistor arranged at the n-th stage.

18. A shift register according to claim 17, wherein:

the first power source is a low potential power source;

the second power source is a high potential power source;

the first transistor and the fifth transistor are each an N-type transistor; and

the second to fourth transistors are each a P-type transistor.

19. A shift register according to claim 17, wherein:

the first power source is a high potential power source;

the second power source is a low potential power source;

the first transistor and the fifth transistor are each a P-type transistor; and

the second to fourth transistors are each an N-type transistor.

20. A shift register according to claim 17, wherein the fourth transistor is replaced with an analog switch.

21. A shift register according to claim 17, wherein the second transistor is eliminated.

22. A shift register comprising:

a plurality of stages each of which includes: a first clocked inverter including a first transistor and a second transistor connected in series; an inverter that forms a loop with the first clocked inverter; and a compensation circuit including an N-type transistor and an analog switch, wherein:

the first transistor is a P-type transistor and the second transistor is an N-type transistor;

a gate of the first transistor is connected to an output terminal of the inverter and a source of the first transistor is electrically connected to a high potential power source;

a gate of the second transistor is connected to a clock signal line through a drain of the N-type transistor and the analog switch and a source of the second transistor is connected to a low potential power source; and

the analog switch is controlled by input into and output from the inverter.

23. A shift register comprising:

a plurality of stages each of which includes: a first clocked inverter including a

first transistor and a second transistor connected in series; an inverter that forms a loop with the first clocked inverter; and a compensation circuit including a P-type transistor and an analog switch, wherein:

the first transistor is an N-type transistor and the second transistor is a P-type transistor;

a gate of the first transistor is connected to an output terminal of the inverter and a source of the first transistor is electrically connected to a low potential power source;

a gate of the second transistor is connected to a clock signal line through a drain of the P-type transistor and the analog switch and a source of the second transistor is connected to a high potential power source; and

the analog switch is controlled by input into and output from the inverter.

24. A clocked inverter comprising:

a first transistor and a second transistor connected in series, and

a compensation circuit comprising a third transistor and a fourth transistor connected in series, wherein:

gates of the third transistor and the fourth transistor are connected to each other,

drains of the third transistor and the fourth transistor are each connected to a gate of the first transistor,

sources of the first transistor and the fourth transistor are each electrically connected to a first power source,

a source of the second transistor is electrically connected to a second power source.

25. A shift register comprising:

a first compensation circuit inputted a first signal;

a second compensation circuit inputted a second signal;

a first clocked inverter electrically connected with the first and second compensation circuits;

a third compensation circuit comprising a first analog switch, inputted the first signal;

a fourth compensation circuit comprising a second analog switch, inputted the second signal;

a second clocked inverter electrically connected with the third and fourth compensation circuits.